CERTIFICATE OF VERIFICATION

I, Myung Suk LEE, of 648-23 Yeoksam-dong, Kangnam-ku, Seoul, Korea state that the attached document is a true and complete translation to the best of my knowledge of the Korean-English language and that the writings contained in the following pages are correct English translation of the specification and claims of the Korean Patent Application No. P1996-73475.

Dated this 18th day of April, 2003.

Signature of translator: Myungsuk Lee

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[ABSTRACT OF THE DISCLOSURE] 96-73475

[ABSTRACT]

Semiconductor device in which a method for forming a self-aligned contact hole is used to achieve a contact hole of a good reliability is disclosed, the method for forming a method for forming a contact hole of a semiconductor device including the steps of: successively forming a gate insulating layer and a conductive layer with a gate cap insulating layer on a semiconductor substrate; forming a first impurity region under surface of the semiconductor substrate at both sides of the conductive layer; forming an interlayer insulating layer on the semiconductor substrate inclusive of the conductive layer; selectively etching the interlayer insulating layer, the gate insulating layer and the gate cap insulating layer so as to divide the conductive layer into two conductive patterns; forming a second impurity region under the surface of the semiconductor substrate of the conductive layer etched; forming insulating sidewalls on the sides of the conductive pattern divided and the interlayer insulating layer; and forming a conductive region so as to contact the second impurity region.

[TYPICAL DRAWING]

FIG. 5D

[INDEX]

gate cap insulating layer, gate insulating sidewall, field oxide layer, bit line

[SPECIFICATION]

[TITLE OF THE INVENTION]

METHOD FOR FORMING A CONTACT HOLE OF A SEMICONDUCTOR DEVICE

[BRIEF DESCRIPTION OF THE DRAWINGS]

Figs. 1a to 1c are cross-sectional views showing a conventional method for forming a contact hole of a semiconductor device;

Figs. 2a to 2c are cross-sectional views showing another conventional method for forming a contact hole of a semiconductor device;

Fig. 3 is a cross-sectional view showing problems of a structure of the conventional method according to Figs. 2a to 2c;

Fig. 4 is a plain view of a semiconductor device according to the invention; and

Figs. 5a to 5d are cross-sectional views showing a method for forming a contact hole of a semiconductor device according to a preferred embodiment of the invention.

Description of reference numerals for main parts in the drawings

30. substrate	31. field oxide layer
32. gate oxide layer	33. conductive line
33a. first gate line	33b. second gate line
34. gate cap insulating layer	35. first source/drain region
36. gate insulating sidewall	37. interlayer insulating layer
38. photoresist layer	39. second source/drain region
40. oxide sidewall	41. bit line

[DETAILED DESCRIPTION OF THE INVENTION]

[OBJECT OF THE INVENTION]

[FIELD OF THE INVENTION AND DISCUSSION OF THE RELATED ART]

The present invention relates to a semiconductor device and, more particularly, to a method for forming a contact hole of a semiconductor device in which a self-aligned contact hole is formed to achieve a good reliability.

Discussion of the Related Art

The present invention relates to a semiconductor device and, more particularly, to a method for forming a contact hole of a semiconductor device in which a self-aligned contact hole is formed to achieve a good reliability.

A general process of forming a self-aligned contact hole, in which a fine pattern can be easily, precisely made, does not require any location-fitting margin for fitting a mask. Accordingly, a high integration can be achieved without utilizing a highly skilled technique or an equipment of a high preciseness.

There are two conventional methods for forming a self-aligned contact hole. In one of the two method, selective etch rates are used. In the other method, which is a semi self-alignment method, a contact hole is formed and then an oxide sidewall is formed.

In a conventional method for forming a contact hole of a semiconductor device will be explained with reference to the accompanying drawings.

Figs. 1a to 1c are cross-sectional views showing a method for forming a contact hole of a semiconductor device and Figs. 2a to 2c are cross-sectional views showing another method for forming a contact hole of a semiconductor device. Through Fig. 3 which is a cross-sectional view showing a structure of a contact hole of a semiconductor device manufactured according to a conventional method, there can be found problems of a conventional semiconductor device.

Referring initially to Fig. 1a, an active region and a field region are defined on a

substrate 1 and then a field oxide layer is formed on the field region. Next, an oxide layer, a polysilicon layer, and a nitride layer are successively formed on the entire surface. Subsequently, a photoresist layer is coated on the entire surface and then is subjected to exposure and development to be selectively patterned. With the photoresist pattern serving as a mask, the nitride layer, the polysilicon layer, and the oxide layer are successively etched to form a gate oxide layer 2, a gate electrode 3, a gate cap insulating layer 4. Thereafter, the remaining photoresist layer is removed.

With the gate electrode 3 serving as a mask, lightly doped impurity ions are implanted into the exposed surface of the substrate 1, thus forming lightly doped source and drain regions 5. Next, a nitride layer is deposited on the entire surface and then is anisotropically etched to form insulating sidewalls 6 on both sides of the gate electrode 3. With the gate electrode 3 and the gate insulting sidewalls 6 serving as masks, heavily doped impurity ions are implanted into the exposed surface of the substrate 1, thus forming a heavily doped source/drain region 7.

Referring to Fig. 1b, on the entire surface, there is formed an interlayer insulating layer 8 on which a photoresist layer 9 is formed and then patterned with a process of exposure and development.

Referring to Fig. 1c, with the photoresist pattern 9 serving as a mask, the interlayer insulating layer 8 is anisotropically etched using a high selective etch rate of the oxide and nitride layers until the surface of the substrate 1 is exposed, thus forming a contact hole. Next, on the entire surface, there is formed a conductive material such as polysilicon, aluminum, or tungsten and then patterned to form a bit line 10.

Another conventional method for forming a contact hole of a semiconductor device will be explained with reference to the accompanying drawings.

Referring initially to Fig. 2a, on a substrate 11, there are defined an active region and a field region. A field oxide layer is formed on the field region. Then, a first oxide layer, a polysilicon layer, and a second oxide layer are successively formed on the entire surface. Subsequently, a photoresist layer is coated on the entire surface and then is subjected to exposure and development to be patterned. With the photoresist pattern serving as a mask, the first oxide layer, the polysilicon layer, and the second oxide layer are successively etched to form a gate oxide layer 12, a gate electrode 13, and a gate cap insulating layer 14 on a predetermined portion of the substrate 11. Thereafter, the remaining photoresist layer is removed.

With the gate electrode 13 serving as a mask, lightly doped impurity ions are implanted into the exposed surface of the substrate 11, so as to form lightly doped source and drain regions 15. Next, an oxide layer is formed on the entire surface and then is anisotropically etched to form gate insulating sidewalls 16 on both sides of the gate electrode 13. With the gate electrode 13 and the gate insulating sidewalls 16 serving as masks, heavily doped impurity ions are implanted into the substrate 11, thus forming a heavily doped source/drain region 17.

Referring to Fig. 2b, on the entire surface, there is deposited an interlayer insulating layer 18 with a chemical vapor deposition (CVD) method. Next, a photoresist layer 19 is coated on the entire surface and then subjected to exposure and development to be selectively patterned.

Referring to Fig. 2c, with the photoresist pattern 19 serving as a mask, the interlayer insulating layer 18 is anisotropically etched to expose the surface of the source/drain region 17, thus forming a contact hole. Then, an oxide layer is formed on the entire surface and then is anisotropically etched to form oxide sidewalls 20 on both sides of the gate electrode

13 and the bit line 21. Subsequently, a conductive material such as polysilicon, aluminum, or tungsten is formed on the entire surface and then is patterned, thereby forming a bit line 21. In this case, the oxide sidewalls 20 serve to insulate the gate electrode 13 from the bit line 21.

Next, problems of a contact hole of semiconductor devices manufactured according to a conventional method will be explained with reference to the drawing.

As shown in Fig. 3, in case an alignment tolerance is behind the limit of photolithography process, a contact hole is aligned on a gate electrode 13, so as to form a step on the gate electrode 13, so that a short between the gate electrode 13 and the bit line 21 is generated after the formation of the oxide sidewalls 20.

[TECHNICAL TASKS TO BE ACHIEVED BY THE INVENTION]

However, conventional methods for forming a contact hole of a semiconductor device have the following problems.

First, it is difficult to carry out an etch process over materials such as a nitride and an oxide having a high etch selective etch rate. If an etch selective rate is high, a polymer can be generated such that a contact hole can be blocked and such that the etch process may be stopped. Moreover, it is difficult to simplify the overall process.

Second, an aliment tolerance is behind the limit of a photolithography process and thus a misalignment may be generated, such that there may be generated a short between a gate electrode and a bit line, so that a unit device can be destroyed.

Therefore, the present invention is directed to a method for forming a contact hole of a semiconductor device that substantially obviates one or more of problems due to limitations and disadvantages of the related art.

An object of the invention is to provide a method for forming a contact hole of a semiconductor device in which a self-aligned contact hole is formed and an unsymmetrical

device is manufactured.

[PREFERRED EMBODIMENTS OF THE INVENTION]

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, a method for forming a contact hole of a semiconductor device including the steps of: successively forming a gate insulating layer and a conductive layer with a gate cap insulating layer on a semiconductor substrate; forming a first impurity region under surface of the semiconductor substrate at both sides of the conductive layer; forming an interlayer insulating layer on the semiconductor substrate inclusive of the conductive layer; selectively etching the interlayer insulating layer, the gate insulating layer and the gate cap insulating layer so as to divide the conductive layer into two conductive patterns; forming a second impurity region under the surface of the semiconductor substrate of the conductive layer etched; forming insulating sidewalls on the sides of the conductive pattern divided and the interlayer insulating layer; and forming a conductive region so as to contact the second impurity region.

A method for forming a contact hole of a semiconductor device having an aforementioned structure will be explained with reference to the accompanying drawings.

Fig. 4 is a plain view of a semiconductor device and Figs. 5a to 5d are cross-sectional views across line I-I in Fig. 4 showing a method for forming a contact hole of a semiconductor device according to a preferred embodiment of the invention.

Referring initially to Fig. 5a, a field region and an active region are defined on a substrate 30 and then a field oxide layer 31 is formed on the field region. Next, a first thin oxide layer is formed on the entire surface with a chemical vapor deposition (CVD) method and then a polysilicon layer and a second oxide layer are successively formed on the entire surface. In this case, a nitride layer can be deposited instead of the second oxide layer.

Subsequently, the first oxide layer, the polysilicon layer, and the second oxide layer are anisotropically etched to form a gate oxide layer 32, a conductive line 33, and a gate cap insulating layer 34 which have a width of X, as shown in Fig. 4.

Referring to Fig. 5b, with the conductive line 33 serving as a mask, lightly doped impurity ions of an N type are implanted into the substrate 30 of a P type, thus forming first source and drain regions 35. Next, either of an oxide layer or a nitride layer is formed and then is anisotropically etched to form gate insulating sidewalls 36 on the both sides of the conductive line 33.

Referring to Fig. 5c, an interlayer insulating layer 37 of an oxide is formed on the entire surface with a chemical vapor deposition (CVD) method, and then a photoresist layer 38 is coated on the entire surface and is subjected to exposure and development to be selectively patterned.

Subsequently, with the photoresist pattern 38 serving as a mask, the interlayer insulating layer 37 and the conductive line 33 are etched such that the conductive line 33 is divided into two lines, which are a first gate line 33a having a width of X' and a second gate line 33b having a width of X" (See Fig. 4).

Referring to Fig. 5d, the remaining photoresist layer 38 is removed. Impurity ions are implanted into the exposed surface of the substrate 30 between the first and second gate lines 33a and 33b, thus forming a second source/drain region 39. In this case, the second source/drain region 39 has a different ion concentration than the first source/drain region 35 has. The ions of a different concentration are implanted and a thermal diffusion is carried out, thereby manufacturing an unsymmetrical device.

An oxide layer is formed and then is anisotropically etched to form oxide sidewalls 40 on inner sides of the first and second gate lines 33a and 33b and on side surface of the

interlayer insulating layer 37. Subsequently, a conductive material, which is one or more of polysilicon, aluminum, or tungsten, is formed on the entire surface and then is patterned to form a bit line 41, thereby completing the contact hole of a semiconductor device of the invention.

[ADVANTAGES OF THE INVENTION]

A method for forming a contact hole of a semiconductor device of the invention has the following advantages.

First, since oxide sidewalls are formed after dividing a conductive line into two gate lines, and then a sidewall oxide layer is formed on inner side surface between the two gate line, a contact hole is not formed over the gate lines and there is thus no generation of a short between the gate lines and a bit line. As a result, a device of a good reliability can be manufactured.

Second, a mask to divide the gate electrode can be replaced instead of a mask to define a contact hole. In addition, a process of exposure becomes easy.

Third, first source and drain regions at both sides of the gate line and a second source/drain region are formed respectively by ion implantations of different concentrations, thereby forming an unsymmetrical device.

It will be apparent to those skilled in the art that various modification and variations can be made in the method for forming a contact hole of a semiconductor device of the present invention without departing from the spirit or scope of the inventions. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A method for forming a contact hole of a semiconductor device including the steps of:

successively forming a gate insulating layer and a conductive layer with a gate cap insulating layer on a semiconductor substrate;

forming a first impurity region under surface of the semiconductor substrate at both sides of the conductive layer;

forming an interlayer insulating layer on the semiconductor substrate inclusive of the conductive layer;

selectively etching the interlayer insulating layer, the gate insulating layer and the gate cap insulating layer so as to divide the conductive layer into two conductive patterns;

forming a second impurity region under the surface of the semiconductor substrate of the conductive layer etched;

forming insulating sidewalls on the sides of the conductive pattern divided and the interlayer insulating layer; and

forming a conductive region so as to contact the second impurity region.

2. The method as claimed in claim 1, wherein the conductive layer is formed of a conductive material such as polysilicon, aluminum, or tungsten and is used as a bit line.

3. The method as claimed in claim 1, wherein the insulating sidewall is insulated the etched conductive layer from the conductive region.

4. The method as claimed in claim 1, wherein the first impurity region and the second

impurity region are formed respectively by ion implantations of different concentrations, thereby forming an unsymmetrical device